In the Specification

Please replace the paragraph on page 2 starting on line 8 with the following amended paragraph:

A2

Fig. 1 is an example of a prior art row/column array 1 used to address a unique location.[[.]] The array 1 includes several rows 2 and columns 3. In some instances, an active component, such as a memory cell, a "pixel" for a display screen or a sensor, may be located at the intersection point of a row and a column.

Please replace the paragraph on page 3, starting on line 16 with the following amended paragraph:

A3

Thus, for a square array containing 2^n active elements, $2x2^{n/2}$ lines (i.e., $2^{n/2}$ columns and $2^{n/2}$ rows) must be supplied to and embedded within the array. For example, for an array of 4096 bits (i.e. 2^{12}), 128 (i.e., $2x2^6$) [[)]] lines are necessary, even though the lower limit of binary addresses required from the CPU is only 12 -- a full order of magnitude less than the row/column scheme requires. This disparity grows exponentially as the array grows in size.

Please replace the paragraph on page 10, starting on line 18 with the following amended paragraph:

A4

The combination of storage element 201, addressable switch elements 202 and 204, and feed-throughs may take on ~~may~~ many forms. For instance, the virtual column 200 may include an optical storage element, and optical feed-throughs with electrically controlled addressable switch elements that change in polarization in order to allow the optical information to flow them. Theoretically, the storage elements, addressable switch elements, and feed-throughs may each be electrical elements or optical elements. Thus, there exists a minimum of nine (9) different possible configurations of virtual columns that include a data storage element, each of which is different based on the types of components from which it is constructed. These nine

different possibilities are shown in Table 1 where an "E" represents an electrical element and an "O" represents an optical element.

Please replace the paragraph on page 22, starting on line 32 with the following amended paragraph:

In some embodiments, each signal generator 1202 generates two signals which are different from the two signals generated by every other generator. For instance, signal generator 1202a, which is associated with the first addressable switch element 1204a, may generate light waves having frequencies of 1 and 2 GHz and signal generator 1202b, which is associated with the second addressable switch element 1204b, may generate light waves having frequencies of 3 and 4 GHz. Because each signal generator 1202 may generate unique signals, and addressable switch elements associated with each signal generator are responsive only to the two signals generated by the signal generator, the need to separate the addressing layers described above (or to maintain rigid alignment and registration of the addressable switch elements) becomes moot. Thus, in this embodiment, the matrix as a whole may be made of a clear substance that allows the desired signals to pass there-through. Of course, the substance need not be optically clear, it only needs to be able to pass all of the signals generated by the signal generators 1202.

Please replace the paragraph on page 24, starting on line 4 with the following amended paragraph:

Fig. 14 shows another embodiment by which reading and writing may be effectuated. The embodiment of Fig. 14 includes first and second columns, 1402 and 1404, both of which may operate or be constructed according to any of the embodiments described above. The first column 1402 is coupled to a first flip-flop 1406 and the second column 1404 is coupled to a second flip-flop 1408. In this embodiment, the flip-flops 1406 and 1408 function as storage elements. That is, the flip-flops store the binary data bits associated with each column. The inputs 1412 and 1414 of the first flip flop 1406 may, respectively, be coupled through, for instance, first transistor 1418 and second transistor 1416 to a write line 1420 and a [[read/]]write line 1422. Both the transistors 1416 and 1418 may be coupled to the first column 1402. At least one output of the flip-flops may be coupled to a read-out layer 1410.

Please replace the paragraph on page 26, starting on line 16 with the following amended paragraph:

The first virtual column 1670, assuming that the first signal type is a "1" and the second signal type is a "0" and that the first addressing layer 1602 is provided with the highest order address bit and the sixth addressing layer 1612 with the lowest order address bit, has an address of 101010 and the second virtual column has an address of 100011. The first virtual column 1670 and the second virtual column [[1672]] 1602 both have the highest order bit (i.e., their connection to the first layer 1672) that is responsive to the first signal type. This addressable switch element may thus be thought of as shared between the two virtual columns, 1670 and 1672.

Please replace the paragraph on page 27, starting on line 16 with the following amended paragraph:

Fig. 17b shows another alternative embodiment of a data storage device 1701. In this embodiment, several discrete strips 1710a, 1710b . . . 1710n are placed together. Each discrete strip may include address lines and virtual columns arranged as described above. Each address line may be connected to all of the other lines that are on the same level. For instance, the top address line 1712a of the first strip 1710a may be connected to the top address line 1712b of strip 1710b. The connection may be through the strips by utilizing feed-throughs or via an external connection such as a wire or by direct contact ~~and or~~ and/or subsequent fusion into a contiguous layer.

Please replace the paragraph on page 28 starting on line 1 with the following amended paragraph:

Fig. 18 shows yet another alternative embodiment of a matrix 1800 according to aspects of the present invention. In this embodiment, the matrix 1800 is composed of a plurality of sections 1802a, 1802b . . . 1802n.